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Department of Computer Science and Engineering

COURSE PLAN

Sub.Code	:CS8491	Branch / Year/Sem:	CSE/ II / IV
Sub.Name	: COMPUTER ARCHITECTURE	Batch	: 2018-2022
Staff Name	: Mrs.K.Lalitha	Academic Year	: 2019-2020(Even)

COURSE OBJECTIVE

- To learn the basic structure and operations of a computer.
- To learn the arithmetic and logic unit and implementation of fixed-point and Floating point arithmetic unit.
- To learn the basics of pipelined execution.
- To understand parallelism and multi-core processors.
- To understand the memory hierarchies, cache memories and virtual memories.
- To learn the different ways of communication with I/O devices.

TEXT BOOKS:

1. David A. Patterson and John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Fifth Edition, Morgan Kaufmann / Elsevier, 2014.
2. Carl Hamacher, Zvonko Vranesic, Safwat Zaky and Naraig Manjikian, Computer Organization and Embedded Systems, Sixth Edition, Tata McGraw Hill, 2012.

REFERENCES:

1. William Stallings, Computer Organization and Architecture – Designing for Performance, Eighth Edition, Pearson Education, 2010.
2. John P. Hayes, Computer Architecture and Organization, Third Edition, Tata McGraw Hill, 2012.
3. John L. Hennessey and David A. Patterson, Computer Architecture – A Quantitative Approach||, Morgan Kaufmann / Elsevier Publishers, Fifth Edition, 2012.

WEB RESOURCES

W1. https://d3s.mff.cuni.cz/~ceres/sch/osy/text/index.html
W2. https://en.wikipedia.org/wiki/Instruction_pipelining.
W3. http://www.dauniv.ac.in/downloads/EmbsysRevEd_PPTs/Chap_2Lesson17
W4.http://www.cse.iitm.ac.in/~vplab/courses/comp_org/Input_Output_Organization

CS8491 COMPUTER ARCHITECTURE **L T P C**
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UNIT I BASIC STRUCTURE OF A COMPUTER SYSTEM **9**

Functional Units – Basic Operational Concepts – Performance – Instructions: Language of the Computer – Operations, Operands – Instruction representation – Logical operations – decision making – MIPS Addressing.

UNIT II ARITHMETIC FOR COMPUTERS **9**

Addition and Subtraction – Multiplication – Division – Floating Point Representation – Floating Point Operations – Subword Parallelism

UNIT III PROCESSOR AND CONTROL UNIT **9**

A Basic MIPS implementation – Building a Datapath – Control Implementation Scheme – Pipelining – Pipelined datapath and control – Handling Data Hazards & Control Hazards – Exceptions.

UNIT IV PARALLELISIM **9**

Parallel processing challenges – Flynn‘s classification – SISD, MIMD, SIMD, SPMD, and Vector Architectures – Hardware multithreading – Multi-core processors and other Shared Memory Multiprocessors – Introduction to Graphics Processing Units, Clusters, Warehouse Scale Computers and other Message-Passing Multiprocessors.

UNIT V MEMORY & I/O SYSTEMS **9**

Memory Hierarchy – memory technologies – cache memory – measuring and improving cache performance – virtual memory, TLB‘s – Accessing I/O Devices – Interrupts – Direct Memory Access – Bus structure – Bus operation – Arbitration – Interface circuits – USB.

TOTAL : 45 PERIODS

OUTCOMES:

On Completion of the course, the students should be able to:

- Understand the basics structure of computers, operations and instructions.
- Design arithmetic and logic unit.
- Understand pipelined execution and design control unit.
- Understand parallel processing architectures.
- Understand the various memory systems and I/O communication.

S. No	Topic Name	Books for Reference	Page No	Teaching Methodology	No. of Periods required	Cumulative no. of Periods
UNIT – I BASIC STRUCTURE OF A COMPUTER SYSTEM						
1	Functional Units	T2	3	BB	1	1
2	Basic Operational Concepts	T2	7	BB	1	2
3	Performance	T2	13	BB	1	3
4	Instructions: Language of the Computer	T2	37	BB	1	4
5	Operations Logical operations	T1	121	BB	1	5
6	Operands	T1	66	BB	1	6
7	Instruction representation	T1	80	BB	1	7
8	Decision making	T1	90	BB	1	8
9	MIPS Addressing.	T2	48	BB	1	9
LEARNING OUTCOME At the end of unit, Students should be able to • Discuss trends in Components of a digital computer system. • Demonstrate an understanding of the Instructions in modern computer process. • Understand about Logical operations, control operations in digital computer system.						
UNIT – II ARITHMETIC FOR COMPUTERS						
10	Addition	T1	178	BB	1	10
11	Subtraction	T1	178	BB	1	11
12	Multiplication	T1	183	BB	1	12
13	Division	T1	189	BB	1	13
14	Floating Point Representation	T1	196	BB	1	14
15	Floating Point Operations	T1	196	BB	1	15
16	Floating Point Addition	T1	203	BB	1	16
17	Floating Point Multiplication	T1	206	BB	1	17
18	Subword Parallelism	T1	225	BB	1	18
LEARNING OUTCOME At the end of unit, Students should be able to • To learn and apply the operations of Addition, subtraction, Multiplication, and Division in modern computer. • To learn about floating points operations (add, sub, mul, Div)						

UNIT –III PROCESSOR AND CONTROL UNIT

19	Basic MIPS implementation	T1	244	BB	1	19
20	Logic Design Conventions	T1	248	BB	1	20
21	Building a Datapath	T1	251	BB	1	21
22	Control Implementation Scheme	T1	259	BB	1	22
23	Pipelining	T1	272	BB	1	23
24	Pipelined datapath and control	T1	286	BB	1	24
25	Data Hazards	T1	303	BB	1	25
26	Control Hazards	T1	316	BB	1	26
27	Exceptions.	T1	325	BB	1	27

LEARNING OUTCOME

At the end of unit, Students should be able to

- To learn and apply the operations of MIPS Implementation and control schema implemation.
- To learn about pipeline Hazards and Graphics Processing Units.

UNIT – IV PARALLELISIM

28	Parallel processing challenges	T1	502	BB	1	28
29	Flynn‘s classification	T1	509	BB	1	29
30	Vector Architectures	T1	509	BB	1	30
31	Hardware multithreading	T1	516	BB	1	31
32	Multi-core processors	T1	519	BB	1	32
33	Shared Memory Multiprocessors	T1	519	BB	1	33
34	Introduction to Graphics Processing Units	T1	524	BB	1	34
35	Clusters, Warehouse Scale Computers	T1	531	BB	1	35
36	Message-Passing Multiprocessors	T1	531	BB	1	36

LEARNING OUTCOME

At the end of unit, Students should be able to

- Able to understand Concept of Speculation, Static Multiple Issues.
- Students are able to understand the Hardware multithreading concepts.

UNIT – V MEMORY & I/O SYSTEMS

37	Memory Hierarchy	T1	372	BB	1	37
38	Memory Technologies	T1	378	BB	1	38
39	Cache Memory	T1	383	BB	1	39
40	Measuring and improving cache performance	T1	398	BB	1	40
41	Virtual memory	T1	427	BB	1	41
42	TLB's – Translation Lookaside Buffer	T2	438	BB	1	42
43	I/O Devices,	T2	259	BB	1	43
44	DMA and Interupts	T2	234	BB	1	44
45	Bus operation – Arbitration, USB.	T2	237, 272	BB	1	45

LEARNING OUTCOME

At the end of unit, Students should be able to

- Students are able to understand the memory hierarchy and measuring and improving memory performance.
- Students are able to analyze programmed I/O, I/O processors and DMA and interrupts.

COURSE OUTCOME

At the end of the course, the students will be able to

- Understand the basics structure of computers, operations and instructions.
- Design arithmetic and logic unit.
- Understand pipelined execution and design control unit.
- Understand parallel processing architectures.
- Understand the various memory systems and I/O communication.

INTERNAL ASSESSMENT DETAILS

ASSESSMENT NUMBER	**I**	**II**	**MODEL**
Topic Nos.	1 – 18	19-36	1-45
Date			

ASSIGNMENT DETAILS

ASSIGNMENT	I	II	III
Topic Nos. For Reference	1-18	19-36	37-45
Deadline			

ASSIGNMENT NUMBER	DESCRIPTIVE QUESTIONS / TOPIC (Minimum 8 Pages)
I	1. Explain in detail about the booth algorithms. 2. Explain about addressing mode with neat diagrams.
II	1. Discuss about Data Hazard and Control Hazards. 2. Explain in detail about Pipelining.
III	1. Explain in detail about Parallel Processing challenges.

PREPARED BY
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AP/CSE

VERIFIED BY
HOD/CSE

APPROVED BY
PRINCIPAL